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Hardware and Software Implementation of Median Filter in Image Processing Application

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Abstract

Image can be contaminated in the process of collection, processing and transmission. That's why image de-noising is important part of Image Processing. The existence of Impulse noise in an acquired image is most common problem. Median filter has ability to remove Impulse noise and preserve edges of an image. It is a computationally intensive operation, so processing time of median filter software algorithm is considerably more. Therefore, to meet the real-time filtering requirements, fast hardware based Median filter is used. In this work, median filter is implemented on FPGA and filter quality in terms of Signal-to-noise ratio is measured for several 256 x 256 color (RGB) images.

Keywords: Median Filter; FPGA based Median Filter; Image Processing

Introduction

Image Processing is used in many fields such as medical imaging, robotics and digital camera. In many of these applications due to imperfection of image sensors, images are often corrupted by noise. Impulse noise is most frequently found type of noise. Impulse noise is also caused by malfunctioning pixel in camera sensors, faulty memory in hardware or error in data transmission.

There are mainly two types of impulse noise:-

1. Salt-Pepper noise (intensity spike and speckle noise):- For images corrupted by salt-pepper noise, the noisy pixel can take only maximum and minimum value.
2. Random valued shot noise: - In case of random value shot noise noisy pixels have an arbitrary value.

Salt-pepper noise is characterized by black and white spots on the image. Median filter is very effective in the removal of salt-pepper noise. Median filter also preserves the edges of image during removal of noise. Image signal and existing noise types are usually nonlinear that's why Median filter, being a non-linear filter, is popularly used. Median filter uses sorting algorithm, in which processing time is considerably high. To improve the execution speed of sorting method, we need to use parallel and pipeline approach, which can be achieved by implementing the filter on FPGA (Field Programming Gate Array). Implementing image processing algorithms on reconfigurable device minimizes the time-to-market cost, enables rapid prototyping of complex algorithms and simplifies debugging and verification. Additionally, the reprogrammable feature of FPGA devices provides the user with fast adaptation of the system to ever-changing demands.

Several researchers proposed different methods for hardware implementation of median filter to reduce time and to increase the execution speed. In one of the initial works to introduce novel designs for Median Filter, Gavin Bates et. al. discussed several new designs for FPGA implementation of Median Filter [1].

Building on these multi-stage median filter designs, Miguel A. Vega-Rodríguez, et. al. introduced new architecture and optimizations for implementation of Median Filter with FPGA for meeting real-time requirements [2].

M. Jiang and D. Crookes further extended the systolic array structure based on triple sorting algorithm and proposed high performance architecture of median filter for 3D image de-speckling [3].

Tripti Jain et. al. proposed a reconfigurable FPGA based filter that compared the image filtering speed for 3x3, 5x5 and 7x7 window size for various image sizes [4]. Yan Lu, et. al. suggested optimized sorting algorithm for real time FPGA based median filter of the human visual system [5].

Pingjun Wei, et. al. proposed a fast median filtering algorithm on FPGA that made improvements to conventional median filtering algorithm by adding comparison threshold to further enhance the median filter characteristics of preserving image detail [6].

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Yueli Hu, Huijie Ji et. al. discussed standard and multi-level Median Filters and presented FPGA based solutions for these two [7]. Zdenek Vasicek and Lucas Sekanina proposed a novel hardware implementation for adaptive median filter [8].

Takeaki Metsubara et. al. presented a novel approach having very low computational complexity but still providing superior quality of results in terms of PSNR and image quality for impulse-noise reduction [9].

Carlos R. Castro-Pareja et. al. presented suitable 3D median filter architecture for FPGA that consisted of an ordered semi-systolic array of size equal to the filter window size [10].

It is seen from the referenced research that triple sorting algorithm based on optimized systolic array of comparators is the most efficient and effective technique for hardware implementation of Median Filter. In this work, we have implemented this technique through MATLAB software and also on FPGA Spartan 6 (XC6SLX16) and tested its effectiveness for removal of Salt-and-Pepper noise in wide variety of 256x256 RGB images.

Implementation of Median Filter

Traditional neighborhood averaging filter can suppress isolated out-of-range noise, but the side effect is that it also blurs sudden changes (corresponding to high spatial frequencies) such as sharp edges. The median filter is an effective method that can suppress isolated noise. Specifically, the median filter replaces a pixel by the median of all pixels in the neighborhood:

$$y[m,n]=\text{median}\{x[i,j],(i,j)\in w\} \quad (1)$$

where, w represents a neighborhood centered around location (m, n) in the image.

Median filter is a non-linear filter used in image processing for impulse noise removal during morphological operations, image enhancement and other image processing operations. It finds its typical application in the situations where edges are to be preserved for higher level operations like segmentation, object recognition etc.

Algorithm

Median filter uses sorting algorithm to determine median value of sample window for removal of salt-pepper noise. Common sorting algorithms used for identifying Median are -

a) Bubble Sort
b) Triple (Vertical, Horizontal, Diagonal) Sort

Advanced algorithm, such as Triple Sort, involves sorting the elements of the selected window in three stages viz. rows (vertical sort), columns (horizontal sort) and diagonals. These three stages can be implemented to operate in parallel in hardware. Figure below shows the operation of Triple Sort.

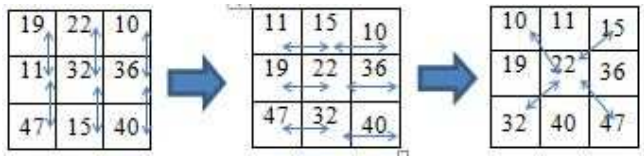

Figure 1 - Median Value using Triple Sort

Software Implementation

The median filtering algorithm described above is implemented using MATLAB. The 3x3 filter window is traversed through the 256x256 image – first along the rows and then along columns and finally along diagonals. Due to the selected filter window size, first row & column and last row & column of the 256x256 image are not filtered. These rows & columns may be ignored or reproduced in filtered image as it is. The resultant filtered image is of size 254x254 pixels. The filtered R, G & B components are stacked together to reconstruct 254x254x3 RGB filtered image copy of the original image.

FPGA Based Median Filter

The architecture of proposed system is shown in the figure below. It consists of UART (Universal Asynchronous Receiver Transmitter) for serial transfer of image pixel data between FPGA kit and personal computer (PC), RAM (Random Access Memory) for storing noisy and filtered image and Median Filter.

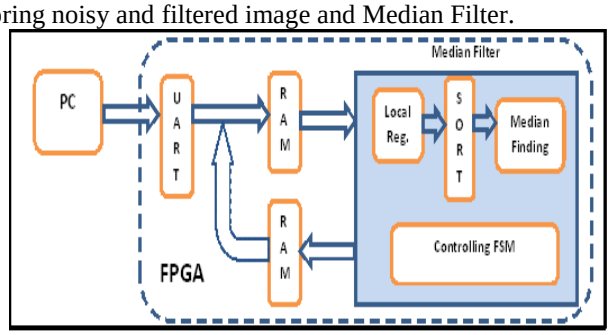

Figure 2 - Median Filter system architecture

The hardware implementation of Median Filter is performed on FPGA Spartan 6 Evaluation Kit (XC6SLX16). Median Filter can be implemented using following two approaches:

a) Comparator based approach
b) Histogram based approach

In this work, comparator based approach is implemented. The design uses optimized systolic array architecture. This architecture comprises of comparator nodes. In this design, the triangular groups with three nodes perform a full sorting on three elements.

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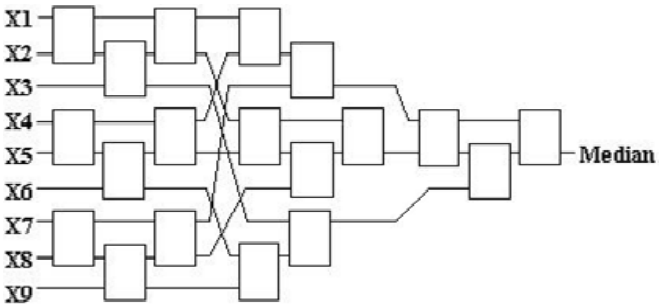

Figure 3 - Comparator based approach for implementing Median filter

For a 3x3 filter window involving 9 8-bit pixel elements, this design needs 19 8-bit comparators and 30 2:1 multiplexers. Each basic node allows sorting of two elements. To do that, each node compares the two elements by means of an 8-bit comparator, using its output in two 2:1 multiplexers.

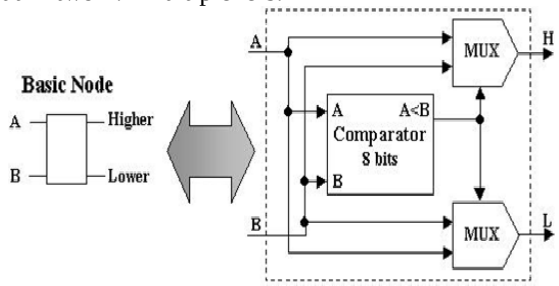

Figure 4 - Basic comparator block

Results

The software and hardware implementation of median filter was tested for several 256x256 RGB images and the effectiveness of noise reduction was measured by comparing the Mean Square Error (MSE), Peak Signal-to-Noise ratio (PSNR) and Signal-to-Noise (SNR) of the noisy and filtered images.

The following set of images shows the comparison of original, noisy, software filtered and hardware filtered images.

Figure 5 - Original Image Apples.bmp

Figure 6 - Noisy Image Apples_Noisy.bmp

Figure 7 - Software filtered image Apples_Filtered.bmp

Figure 8 - Hardware filtered image Apples_HW_Filtered.bmp

The median filter implementations were tested for 36 sample 256x256 RGB images and the MSE, PSNR and SNR of the noisy and filtered images were compared. The charts below show the comparison.

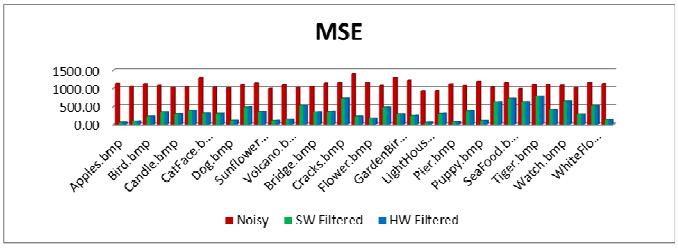

Figure 9 - MSE Comparison of Noisy, SW Filtered and HW Filtered images

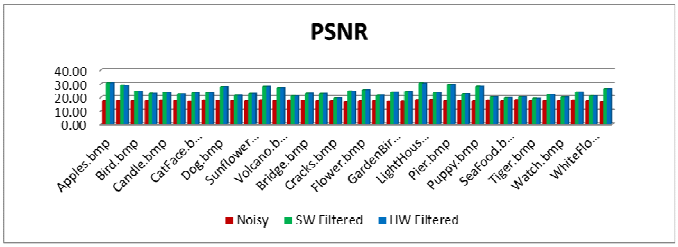

Figure 10 - PSNR Comparison of Noisy, SW Filtered and HW Filtered images

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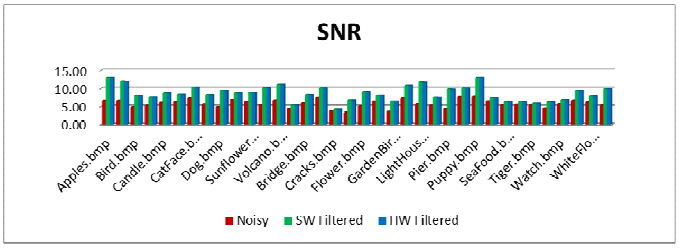

Figure 11 - SNR Comparison of Noisy, SW Filtered and HW Filtered images

Conclusion

In this work, we have implemented median filter in software using MATLAB and in hardware on FPGA Spartan 6 evaluation kit (XC6SLX16). The median filter was tested for several 256x256 RGB images. Filter quality parameters – MSE, PSNR and SNR – were measured and compared for noisy, software filtered and hardware filtered images. The results indicate improvement in MSE, PSNR and SNR of software and hardware filtered images when compared with noisy image. This implementation can be used for designing median filter for image processing chip in mobile and digital cameras.

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